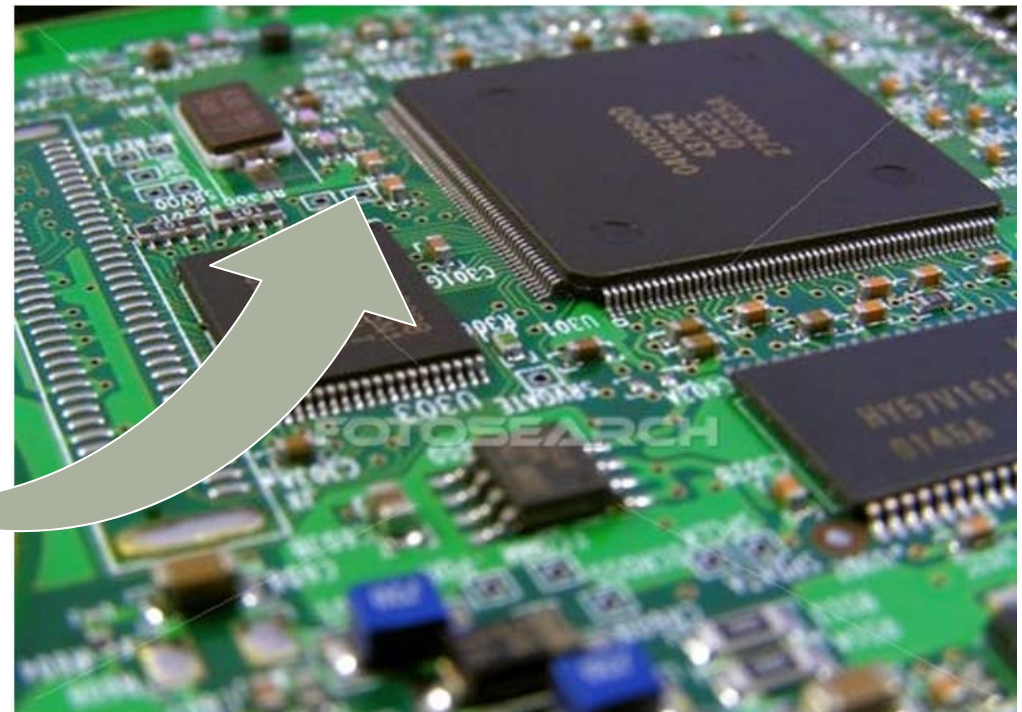
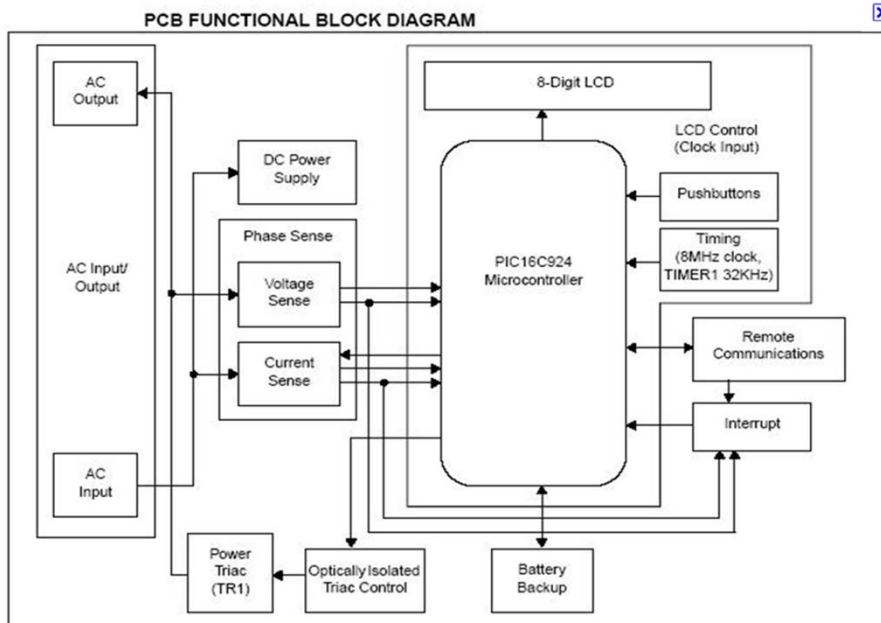




PCB Design Flow

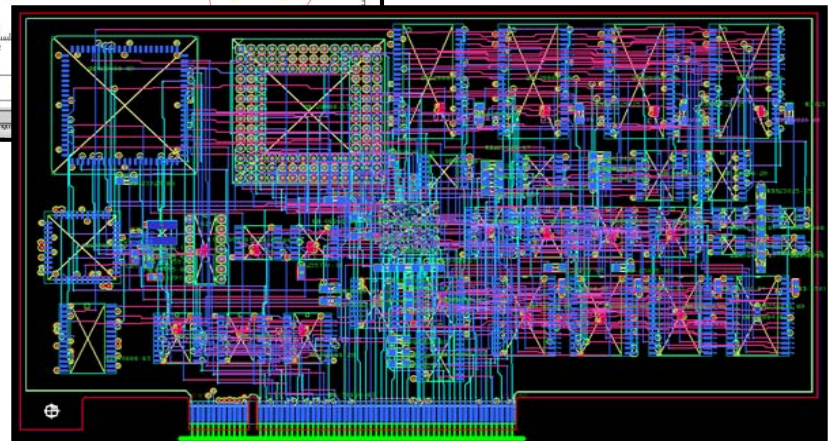
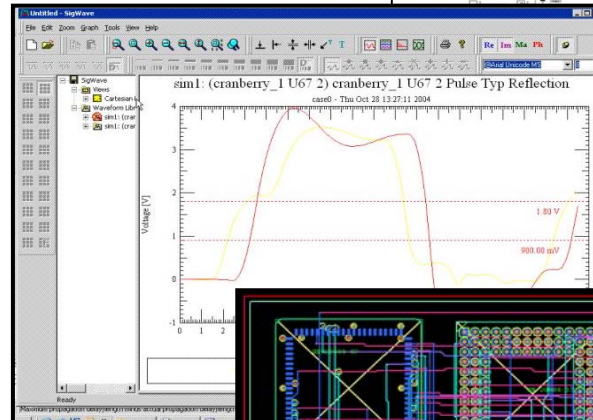
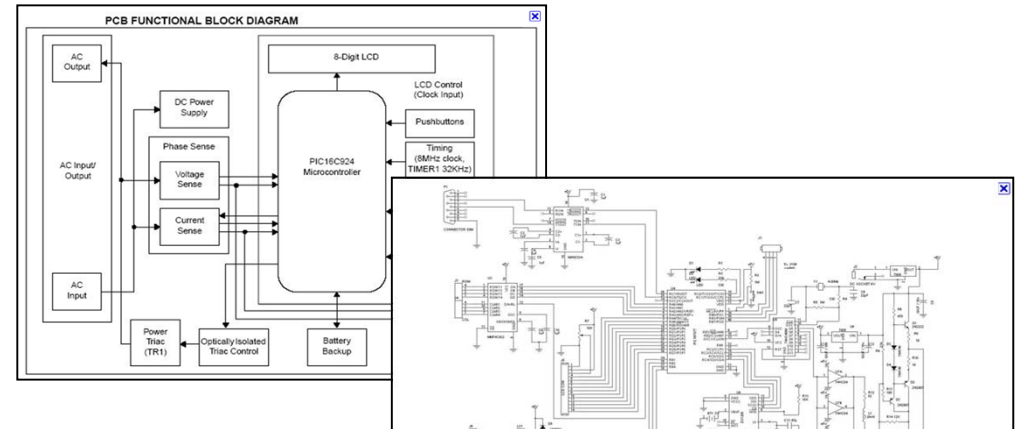
PCB Design Flow



PCB Design Flow Steps



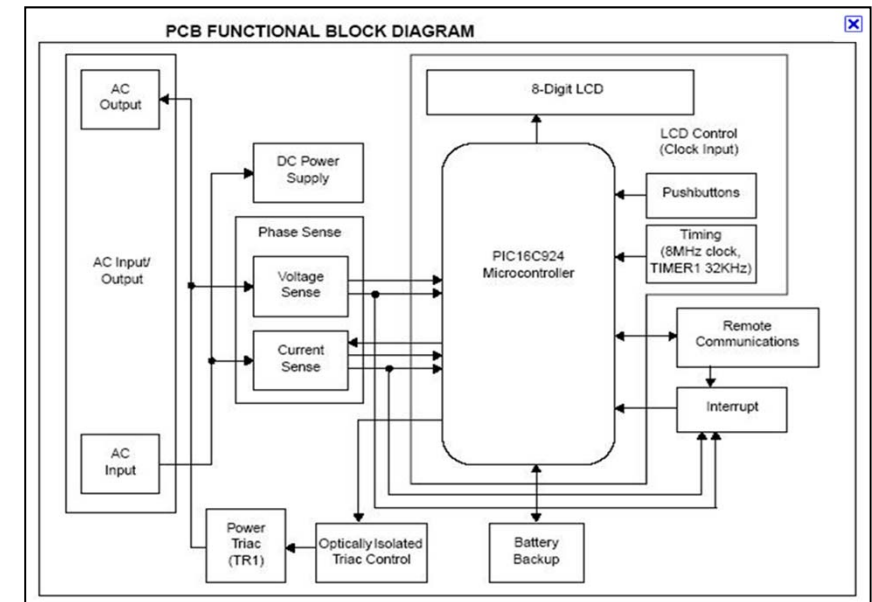
- ✧ Functional Block Diagram
- ✧ Schematic Capture
 - Package Selection
 - Netlist Creation
- ✧ Electrical Simulation
- ✧ Constraint Definition
- ✧ Layout
- ✧ Routing
- ✧ Prototype/Test/Manufacture



Functional Block Diagram



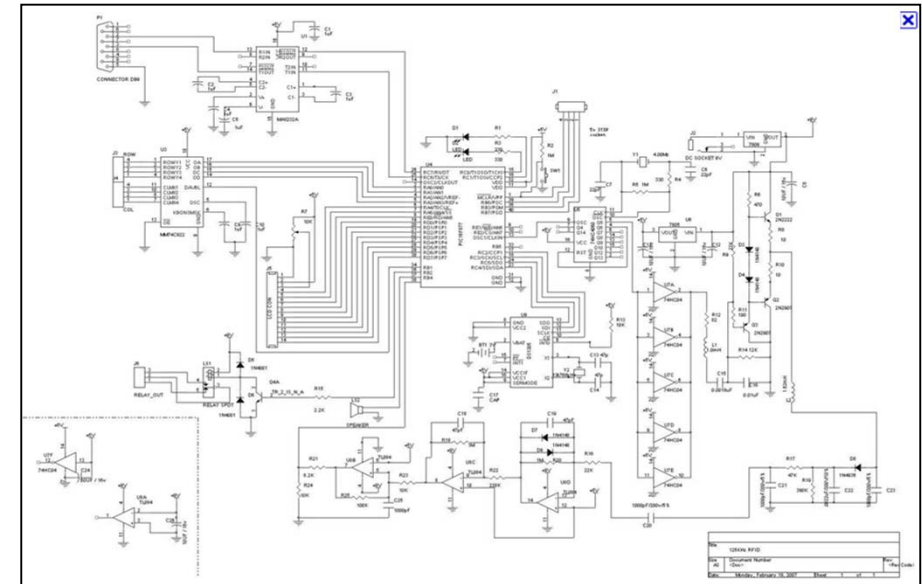
- Architectural description of the functionality required to satisfy market/product requirements
- Part to Part, function to function connectivity
- Little standardization; most common tool is Microsoft Visio



Schematic Capture



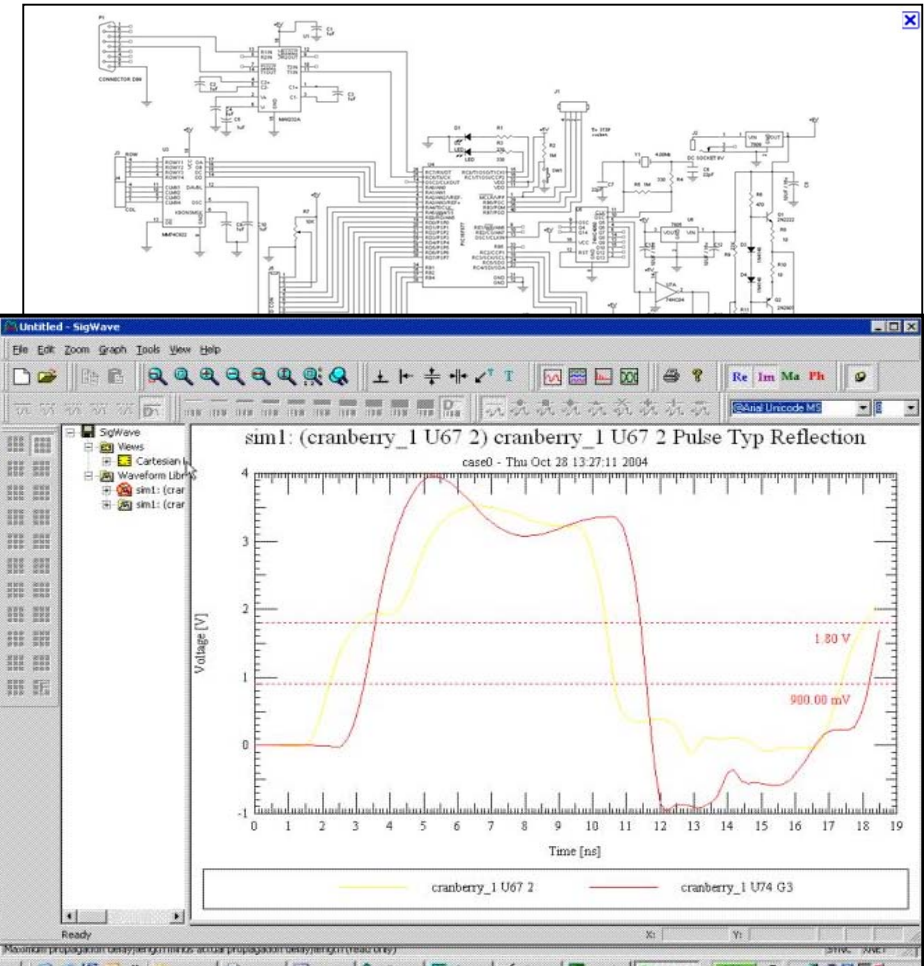
- ✧ Schematic is a circuit diagram
- ✧ Pin to Pin Connectivity is defined for each electrical connection to be made
- ✧ Package Selection occurs here
- ✧ Generation of a net list is a key outcome.
- ✧ Now we have a list of parts, and which pins on those parts must be connected



Electrical Simulation



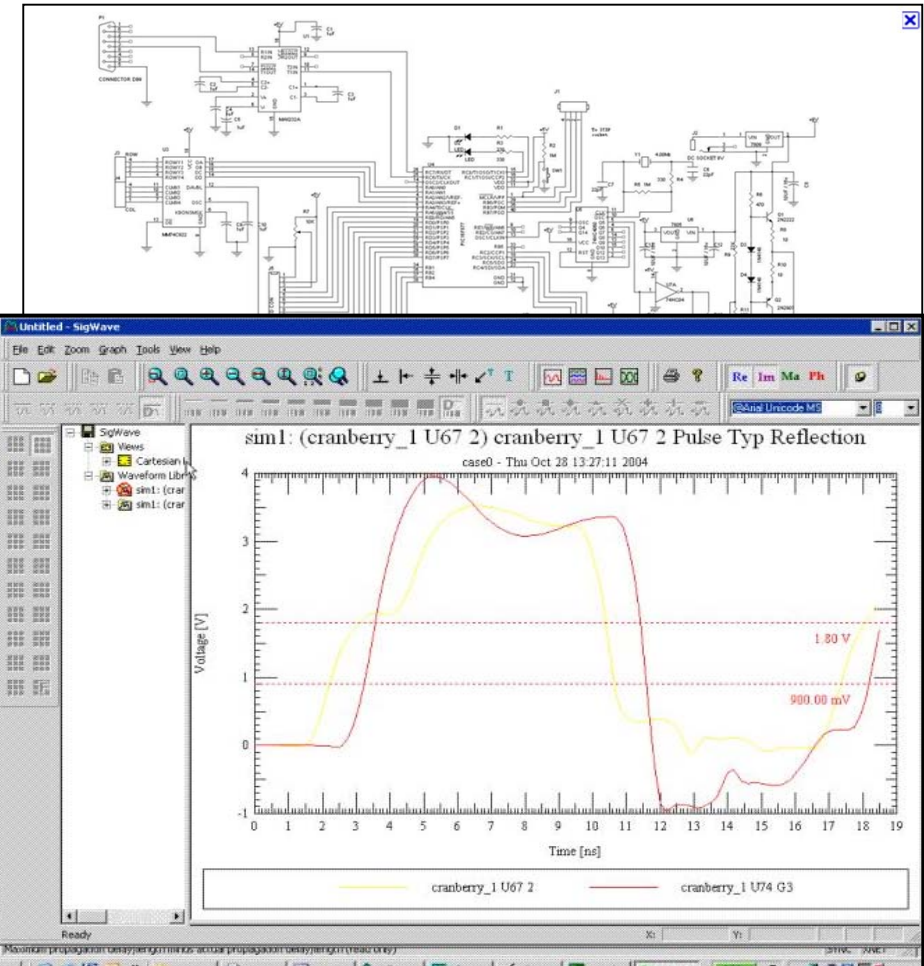
- ∞ Behavioural models of the components (eg, SPICE) can simulate aspects of the virtual circuit
- ∞ Design rules can then be derived from the various results
 - Trace A length must equal Trace B length
 - Trace A length must be less than 1500 mils
 - Trace A width must be > 5 mils
- ∞ Influenced by performance requirements for Signal Integrity (SI), timing



Constraint Entry

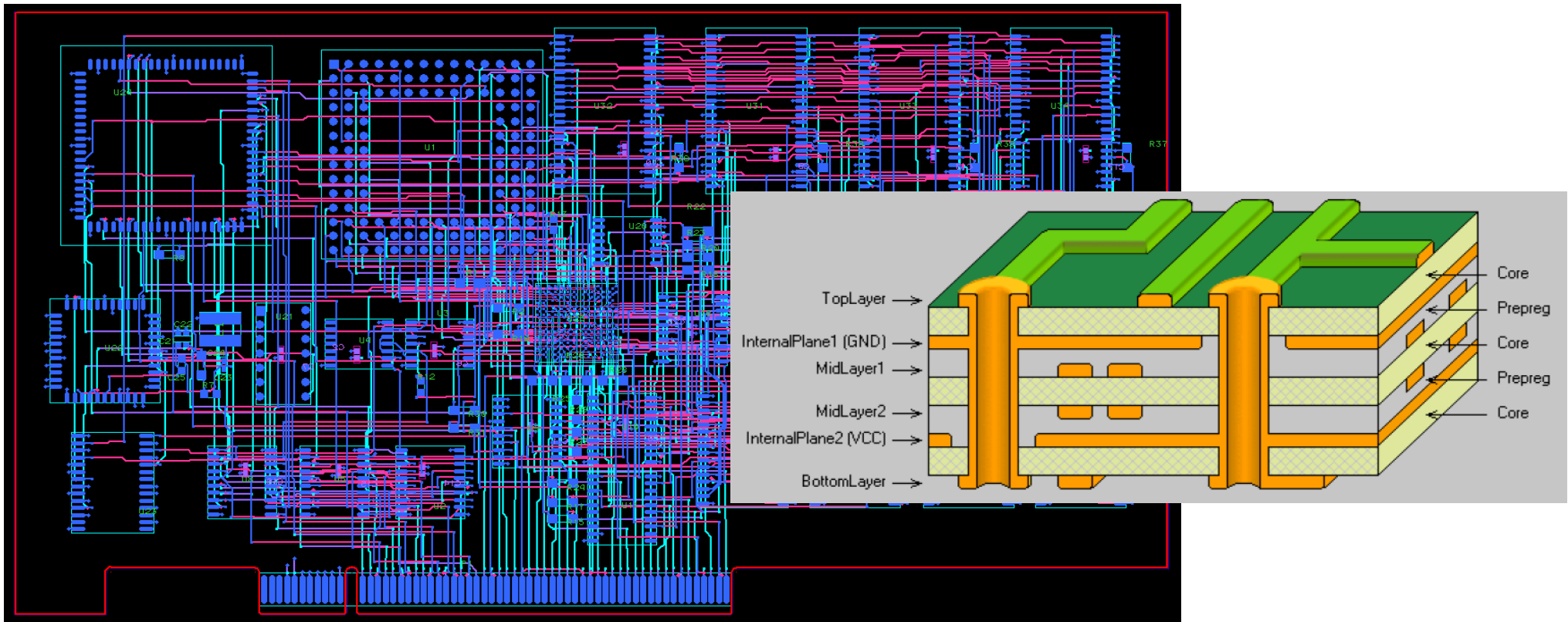


- ∞ The design rules based on electrical performance are combined with other constraints for the PCB design.
- ∞ Manufacturing constraints
 - Trace width
 - Trace spacing
 - Via sizes
- ∞ Mechanical constraints
 - Interferences
 - Board Outline
- ∞ Cost constraints
 - Number of layers
- ∞ The place and route stages are then driven by these constraints and decisions.



Place and Route

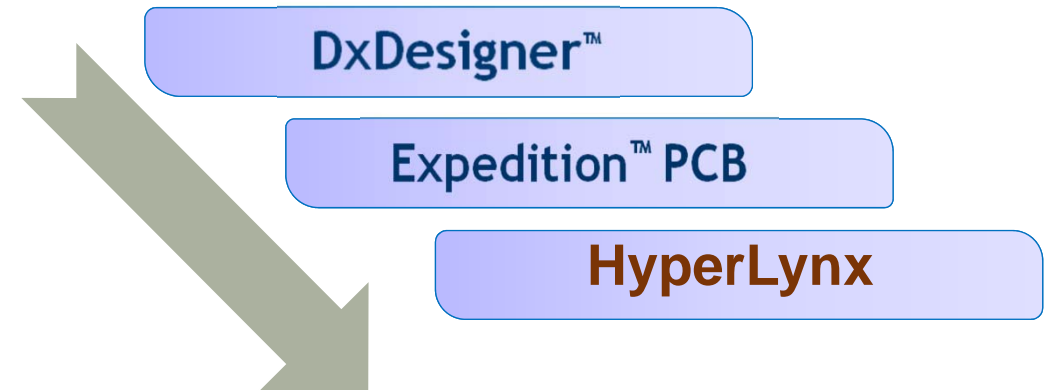
- ✧ The components are placed on the board, and the physical copper pathways to route electrical signals from pin to pin are designed



Mentor Graphics PCB Tools



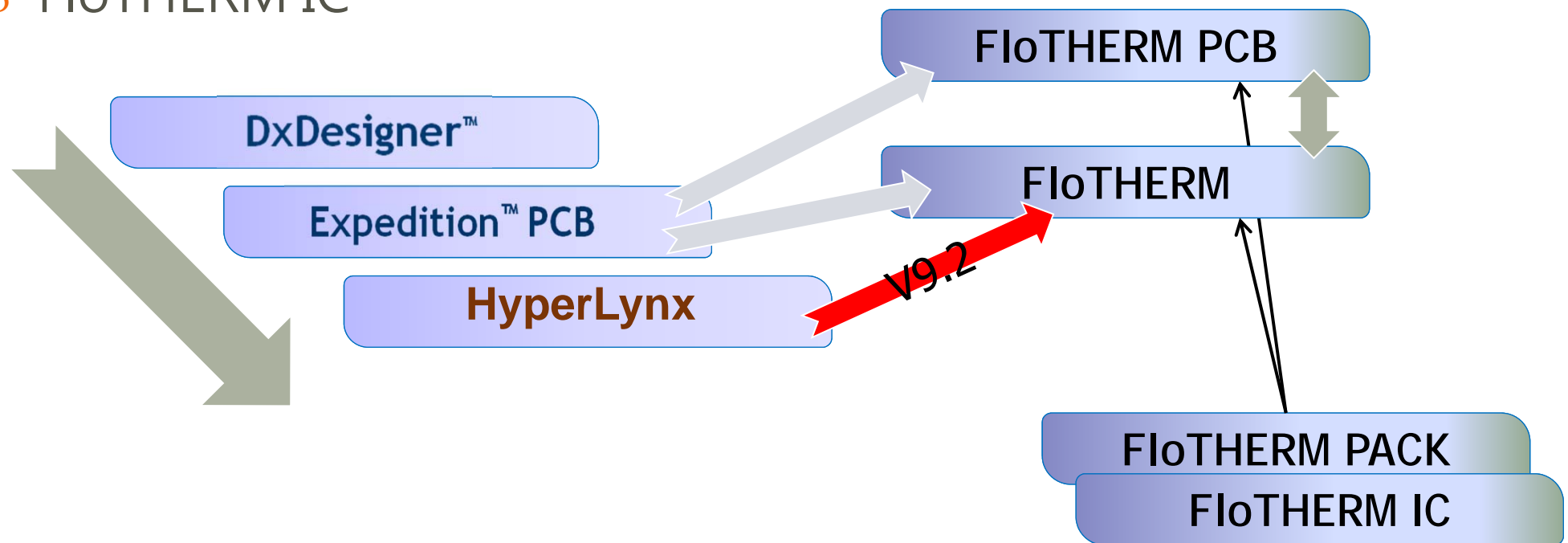
- ∞ Schematic Capture – DxDesigner
- ∞ Constraint Definition – Constraint Editor System
- ∞ Board Layout
 - PADS
 - Boardstation 'Classic'
 - Boardstation XE
 - Expedition PCB
- ∞ Simulation Tools
 - Hyperlynx Power Integrity
 - Hyperlynx Signal Integrity



MAD Tools and Interfaces

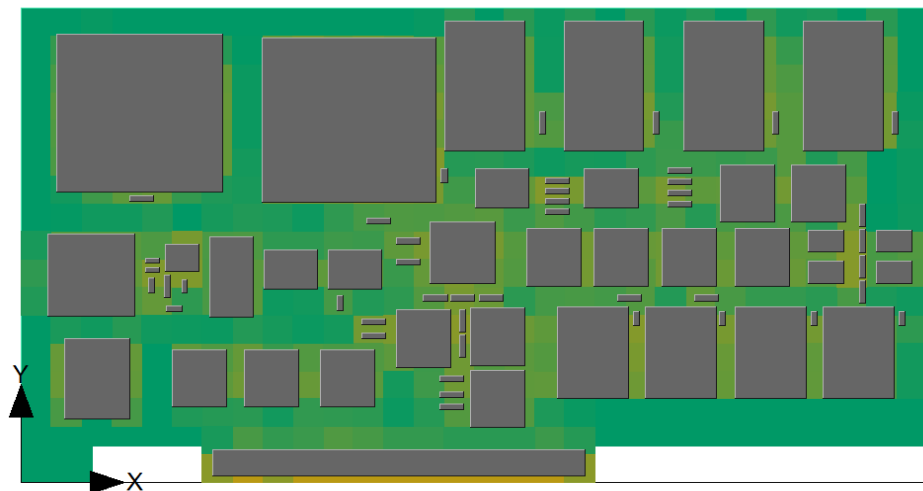
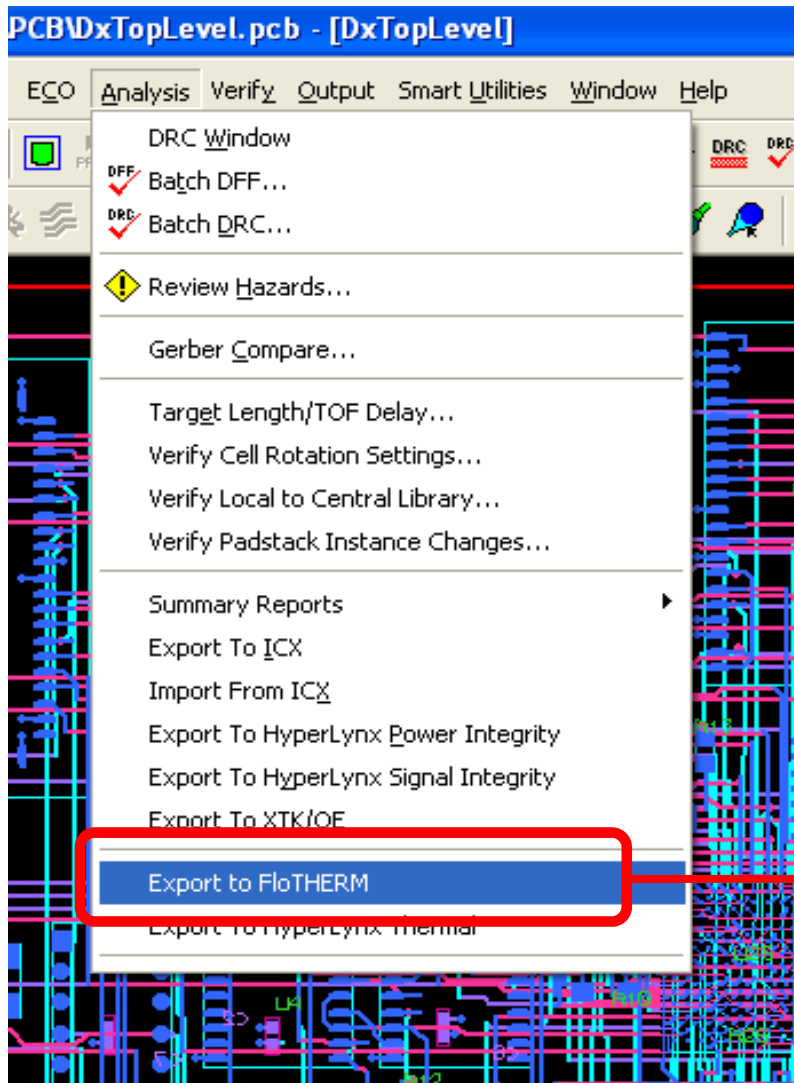


- ∞ FloTHERM
- ∞ FloTHERM PCB
- ∞ FloTHERM PACK
- ∞ FloTHERM IC



Expedition PCB > MAD

- Extracts board outline, component geometry, layer stack up, and metallic distribution
- Imported into FloTHERM or FloTHERM PCB and then prepared for analysis
- Enables an efficient data flow from Expedition PCB to MAD tools, critical to efficiently determining thermal compliance.



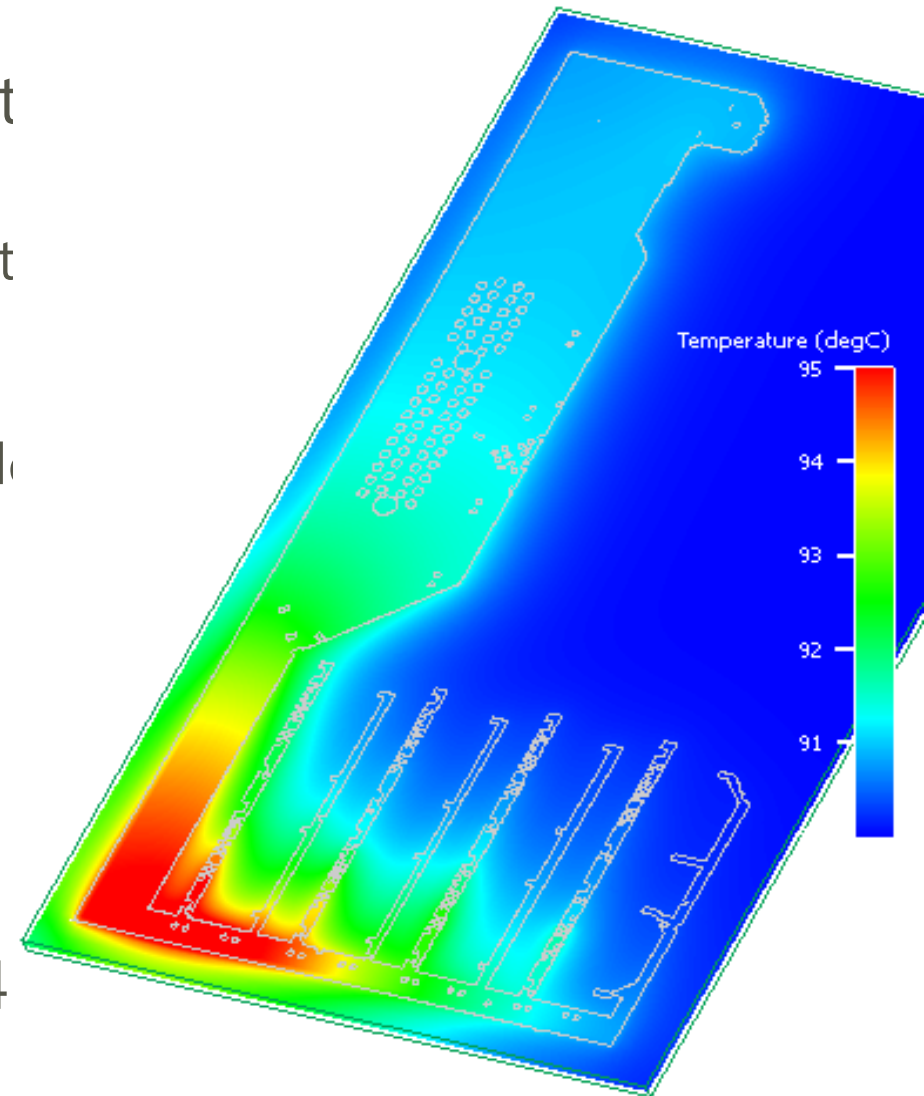
Hyperlynx PI > FloTHERM



∞ DC Drop Joule heating power dissipation taken from HyperLynx PI to FloTHERM

- Detailed net geometry and power density distribution exported after a Power Integrity simulation
- Inserted into an existing FloTHERM model of a PCB
- Resulting temperature prediction takes into account:
 - Net self heating
 - Background heating from actives
 - Effects of the PCB environment

∞ Enabling trace delamination and FR4 melt conditions to be identified



The Unmentioned Constraint - Thermal



- Every bit as important as the previously listed constraints, is that in order to ensure proper and reliable operation, thermal constraints must be met
- Components: Maximum Rated Junction Temperature and/or Maximum Rated Case Temperature
- Board: Maximum allowable temperature for dielectric material

Thermal Specifications

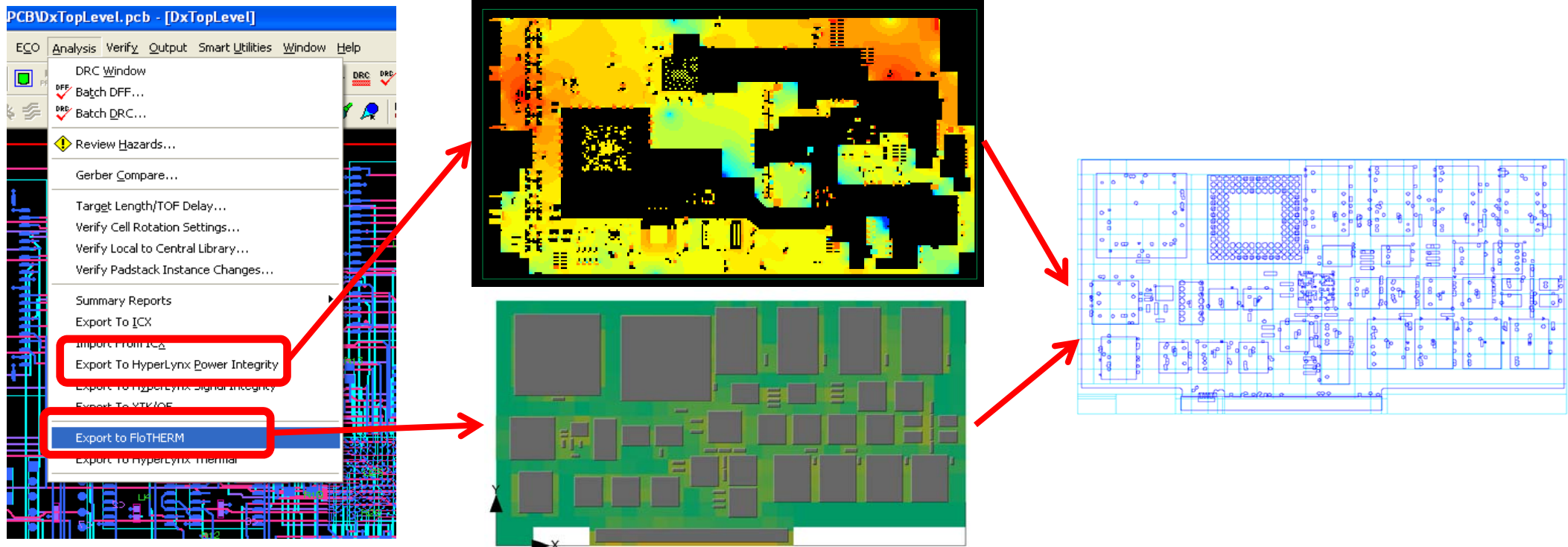
Table 6-2. 64-bit Intel® Xeon™ Processor with 2 MB L3 (PRB = 1)

Power [W]	T _{CASE MAX} [deg C]
P _{CONTROL BASE A} = 27	50
28	51
30	51
32	52
34	52
36	53
38	53
40	54
42	54
44	55
46	56
48	56
50	57

Thermal Design with MAD



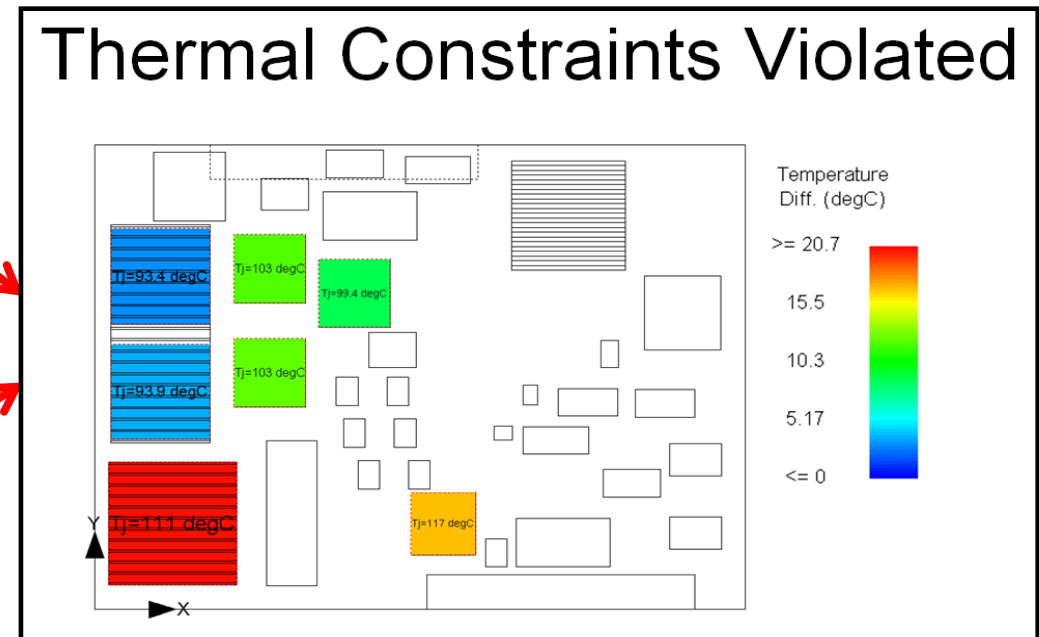
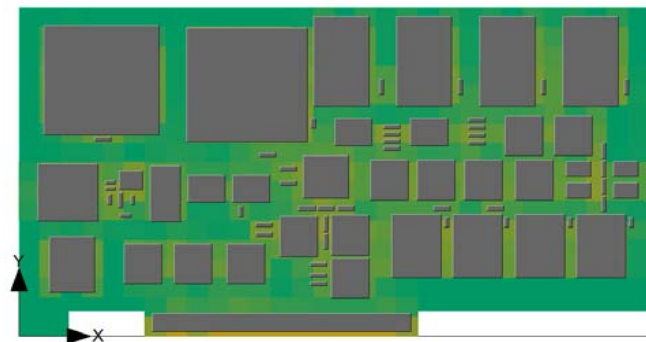
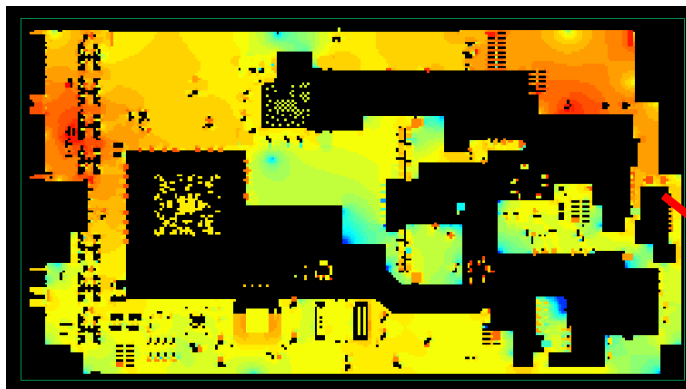
- ✧ Data flow path from Expedition PCB to FloTHERM and FloTHERM PCB better enables concurrent thermal evaluations. Thermal design constraint violations are flagged and designed out.
- ✧ Data flow path from Hyperlynx PI improves the ability of FloTHERM to evaluate additional thermal constraints such as dielectric melt, and trace delamination conditions. Supplement to the Expedition PCB interface.



Thermal Design with MAD



- ∞ Ease of data transfer enables efficient, accurate thermal analysis to be performed in MAD tools.
- ∞ Awareness of thermal constraint margins in the design flow is the result.

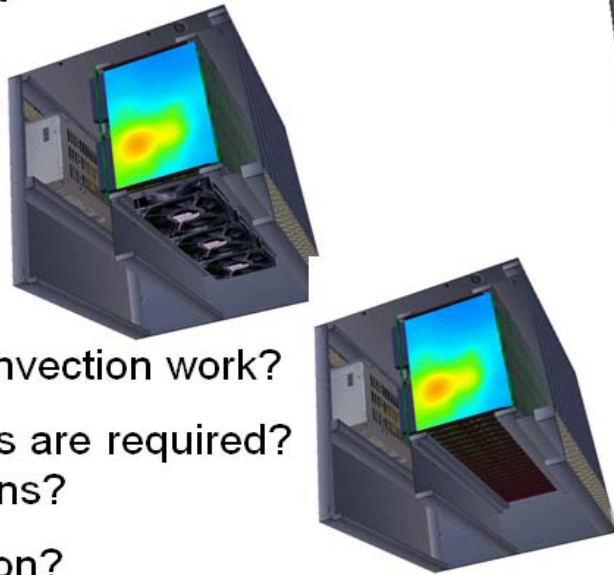


Thermal Design with MAD

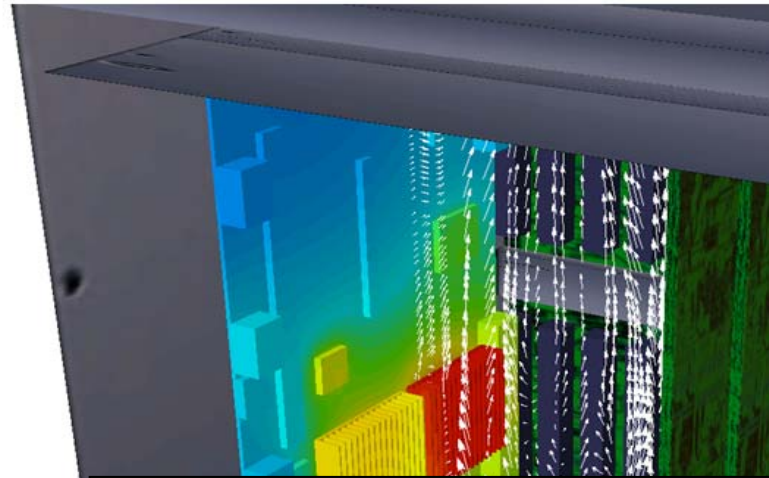


FLOTHERM – Detailed Design Work

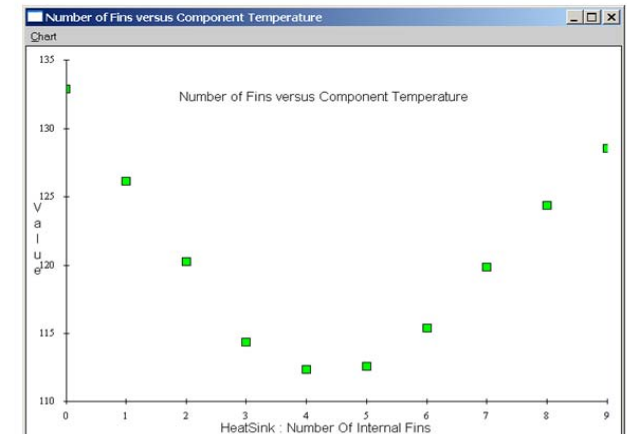
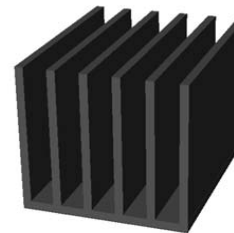
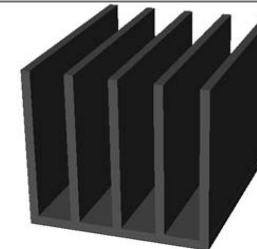
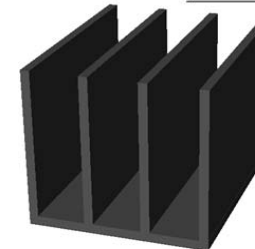
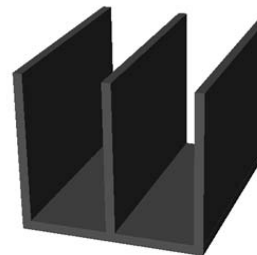
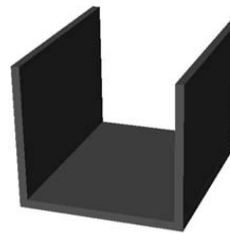
Evaluate different cooling strategies



- Will natural convection work?
- How many fans are required?
What type of fans?
- PCB Distribution?
- Perforated Plate Design?



Parametric Analysis



聯絡我們



- 易富迪科技有限公司
- 台北市松山區南京東路三段 305 號 5F
- 電話：+886-2-87724131
- 傳真：+886-2-27173122
- 網站：www.efd.com.tw
- 客服信箱：CSD@efd.com.tw

