# Managing Temperature Difference Between Critical Components

**IMAPS**

Thermal Management

Los Gatos, California - USA

November 5-7, 2013

# Agenda

- Introduction
- Short History
- Proposed solutions
- Design rules
- Example

# Introduction

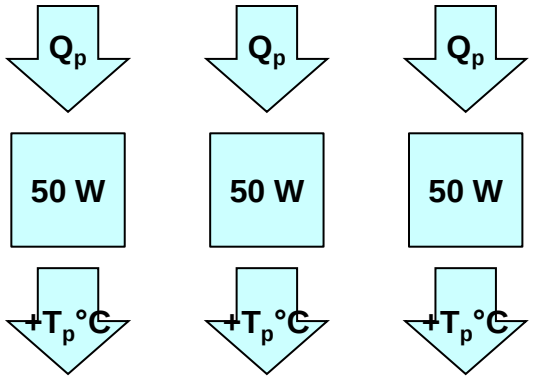
- High performance electronic systems, using parallel circuits or components, require a precise management of parasite capacitors and resistances
- To reach these objectives the components require working at the same temperature
- The constrains between identical components are usually:
  - 0.5 °C difference, expected
  - 1.5 / 2 °C max difference, usually feasible

# Short History

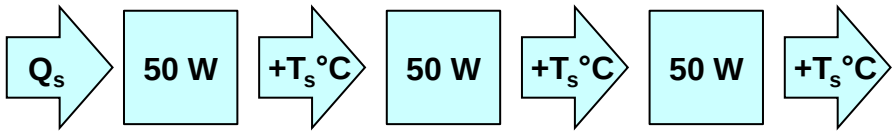
- The standard solution is to have a parallel cooling which means providing the same amount of cooling fluid at the same temperature to each identical component.
  - This solution requires a high flow rate which, in high density system, will be difficult to be pushed inside the system
  - Often preheating due to the complexity of the design might imbalance the temperatures
- Often Engineers prefer to have the components in serial in the cooling scheme. We will therefore observe temperature increases that we can reduce by increasing the flow rate

# Short History

- Parallel Cooling




  - $Q_p$ is going to be 10 g/s for an increase $T_p$ of 5°C : Q total is 30 g/s of air
- Serial Cooling

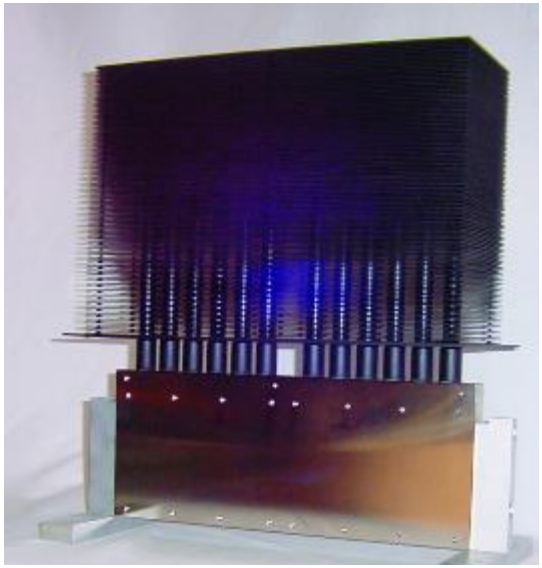



- $Q_s$ is going to be 70 g/s of air for an increase $T_s$ of 1.5 °C before the last chip

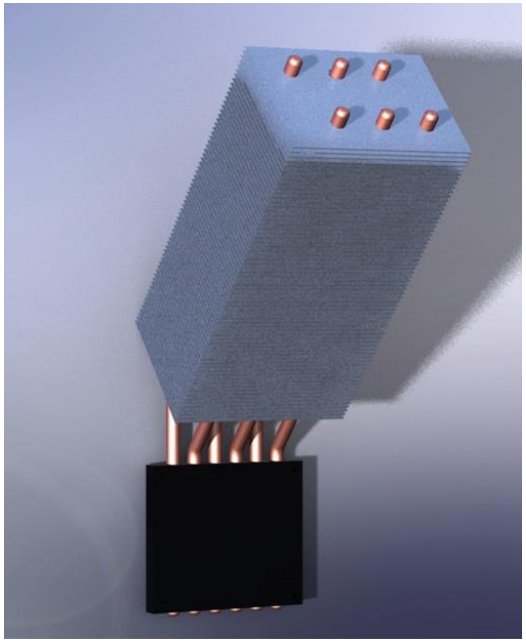
# Short History

- Some advanced solutions are using phase change cooling because the phase change temperature is going to be even over all chips
  - The most common solution is the heat pipe

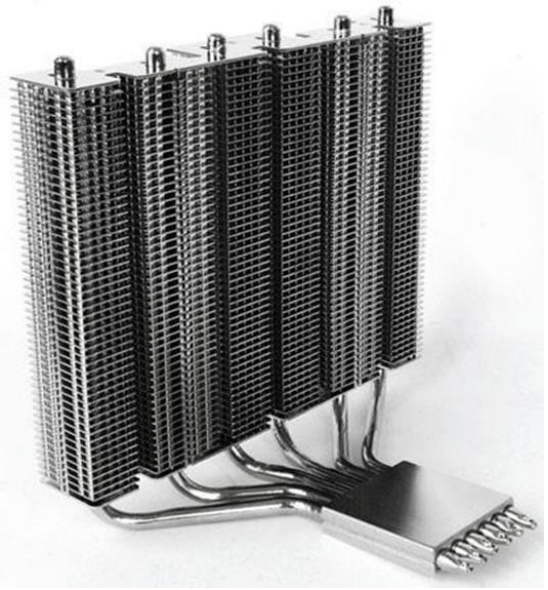
# Short History



Higher pressure drop



Temperature differences created
by the heat exchanger



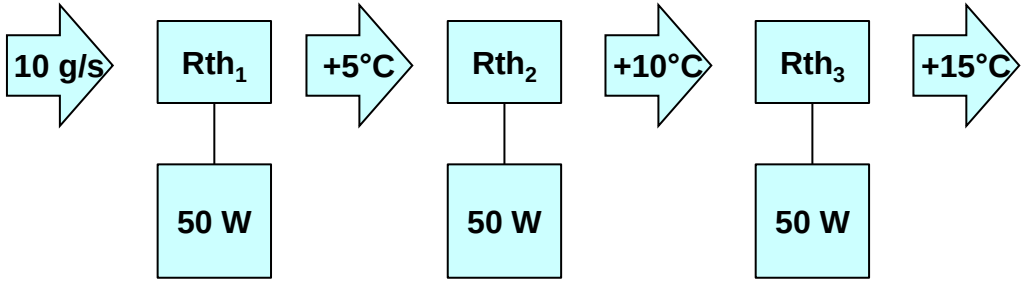
Temperature differences created
by the heat pipe shape

Pictures from Atherm – Schneider/Mersen - Aavid

# Proposed Solutions

- We can satisfy the expectation of Engineers to have a low flow rate, a serial cooling, reduced temperature differences, an optimized pressure drop and low cost by:

**Management of the Rth within the same heat sink**

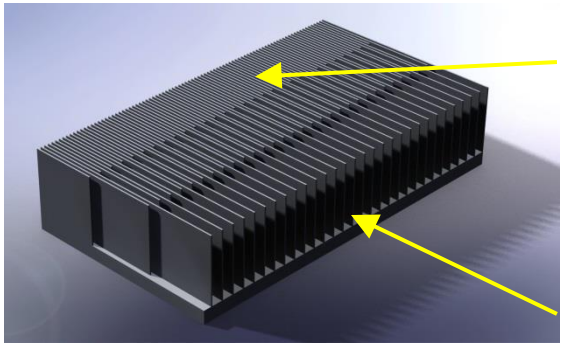



- The only constrain is the proximity of the chips which is often the case to minimize unbalances created by the layout

# Proposed Solutions

- We propose to design only one heat sink:
  - It is a standard solution if the heat sink is an LCP
  - When using air cooling we may design multiple heat sinks with different thermal resistance however:
    - The risk of assembly mistake is high and will be critical for the system
    - The last heat sink will have a higher pressure drop related to the higher fin density requested for reducing the Rth, in this case the air will not go thru the heat sink
- Solutions will look like:

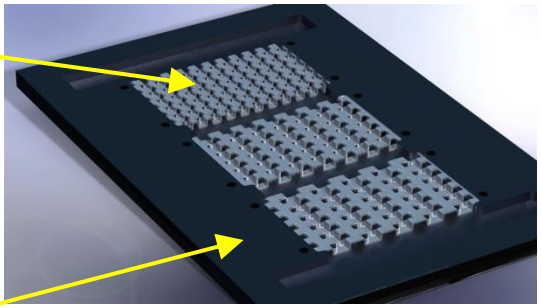
**Air Cooling**



Low Rth

High Rth

**Liquid Cooling Plate**



# Design Process & Rules

- Validate the feasibility of the low Rth heat sink area @ max power ($P_{Max}$ [W or J/S]):
  - Use heat sink data from suppliers: $Rth_{min}$ [°C/W] (@ $Q_{data}$ [kg/s])
- Define input temperature for the last chip (N components):
  - $T_{air\ N\ in}$ [°C] = $T_{case}$ - ($Rth_N$ x $P_{Max}$)
- Define the minimum mass flow @ max power ($P_{Max}$):
  - $Q_{min} = P_{Max} / ( H_c \times ((T_{air\ N\ in} - T_{air\ 1\ in})/(N-1))$
    - $H_c$ is the Heat capacitance of the cooling fluid [J/kg °C]
- Check $Q_{min} > Q_{data}$ if not review $Rth_{min}$ for a higher $Q_{data}$

# Design Process & Rules

- Define Rth heat sink 1 to N-1:
  - $Rth_N = (T_{case} - T_{air\ N\ in}) / P_{Max}$

  Because the $\Delta_T$ out vs. in is about the same (ducted mass flow), Rth increase is equal to
  - $\Delta_{Rth} = \Delta_T / P_{Max}$
  - $Rth_N = Rth_{min} + \Delta_{Rth}\ (N\ (N_{total}\text{-}1)\ T_{case} - T_{air\ N\ in}) / P_{Max}$

- Define local heat sinks:
  - When $\Delta_{Rth}$ is small vs. $Rth_{min}$ we can often only change the heat exchange surface with the fluid proportionally to $\Delta_{Rth}$
  - Of course less surface interacting with the fluid means less pressure drop

# Example

- Single pack IGBT

- 3 modules assembled side by side to manage 3 arms of an inverter, liquid cooled:
  - Max junction temp: 130°C
  - Max case temperature including the thermal interface: 105°C
  - Max fluid temp: 45°C

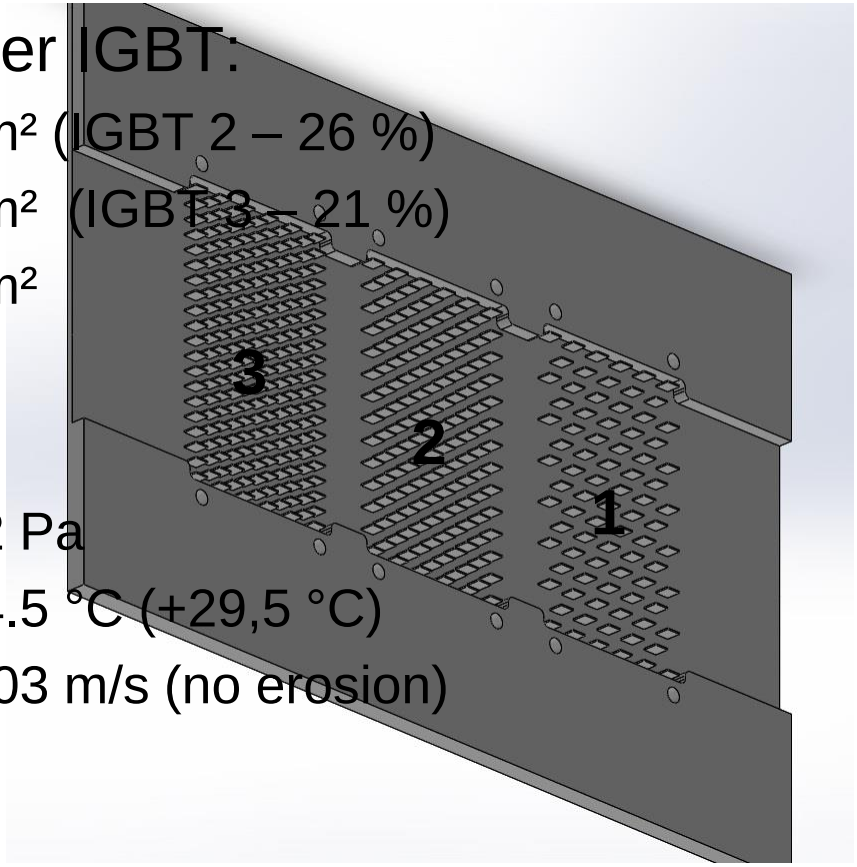
# Example

- Total losses: 1 530 W
  - 510 W per single pack
    - 60 W per IGBT (6x) (50 W/cm²)
    - 25 W per diode (6x) (70 W/cm²)
- Mass flow (water & 30% Glycol):
  - 15 g/s (about 0.8 l/min)
  - $\Delta_T$ = 10°C/IGBT
  - $Rth_{min}$: (105-65) / 510 = 0.08 °C/W (80 °C/kW)
  - $\Delta_{Rth}$ : 10 / 510 = 0.02 °C/W (20 °C/kW)

**$\Delta_{Rth}$ = 25 % of $Rth_{min}$**

# Example

- Heat Exchange surfaces per IGBT:
  - IGBT 1: 9 375 mm² (IGBT 2 – 26 %)
  - IGBT 2: 12 675 mm² (IGBT 3 – 21 %)
  - IGBT 3: 15 975 mm²



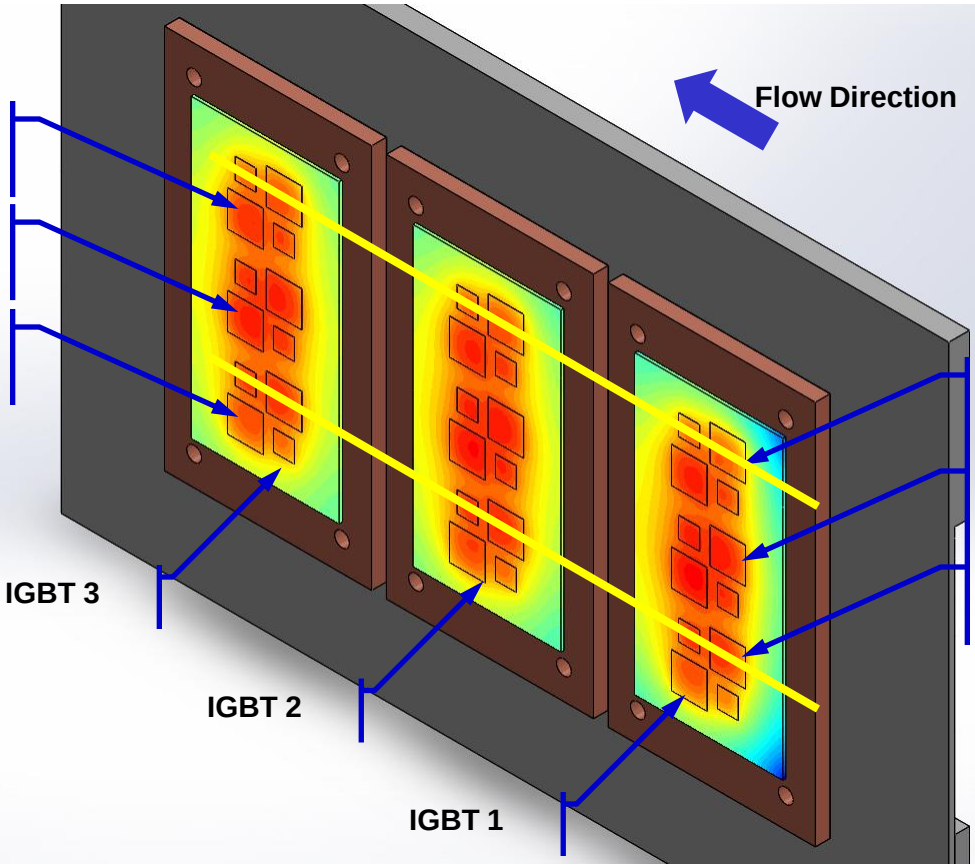

- Simulation results:
  - Max pressure: 22 Pa
  - Fluid exit temperature: 74.5 °C (+29,5 °C)
  - Fluid speed: 0.03 m/s (no erosion)

# Example

Δ IGBT: 1.4 °C
Δ Diode: 1.4 °C

Δ IGBT: 2.1 °C
Δ Diode: 1.2 °C

Δ IGBT: 1.2 °C
Δ Diode: 2.9 °C





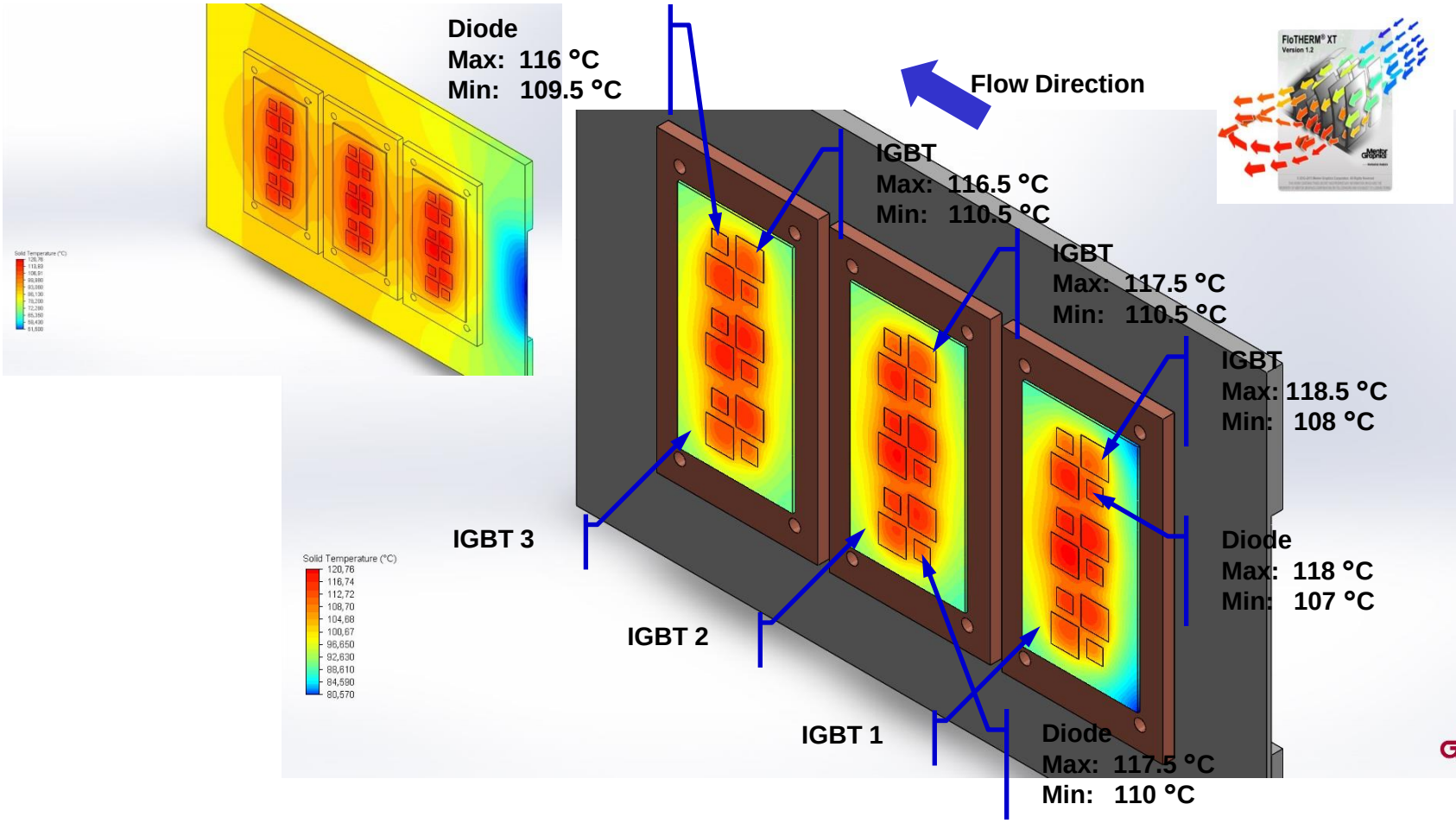
Δ IGBT: 2.6 °C
Δ Diode: 1.4 °C

Δ IGBT: 1.0 °C
Δ Diode: 2.0 °C

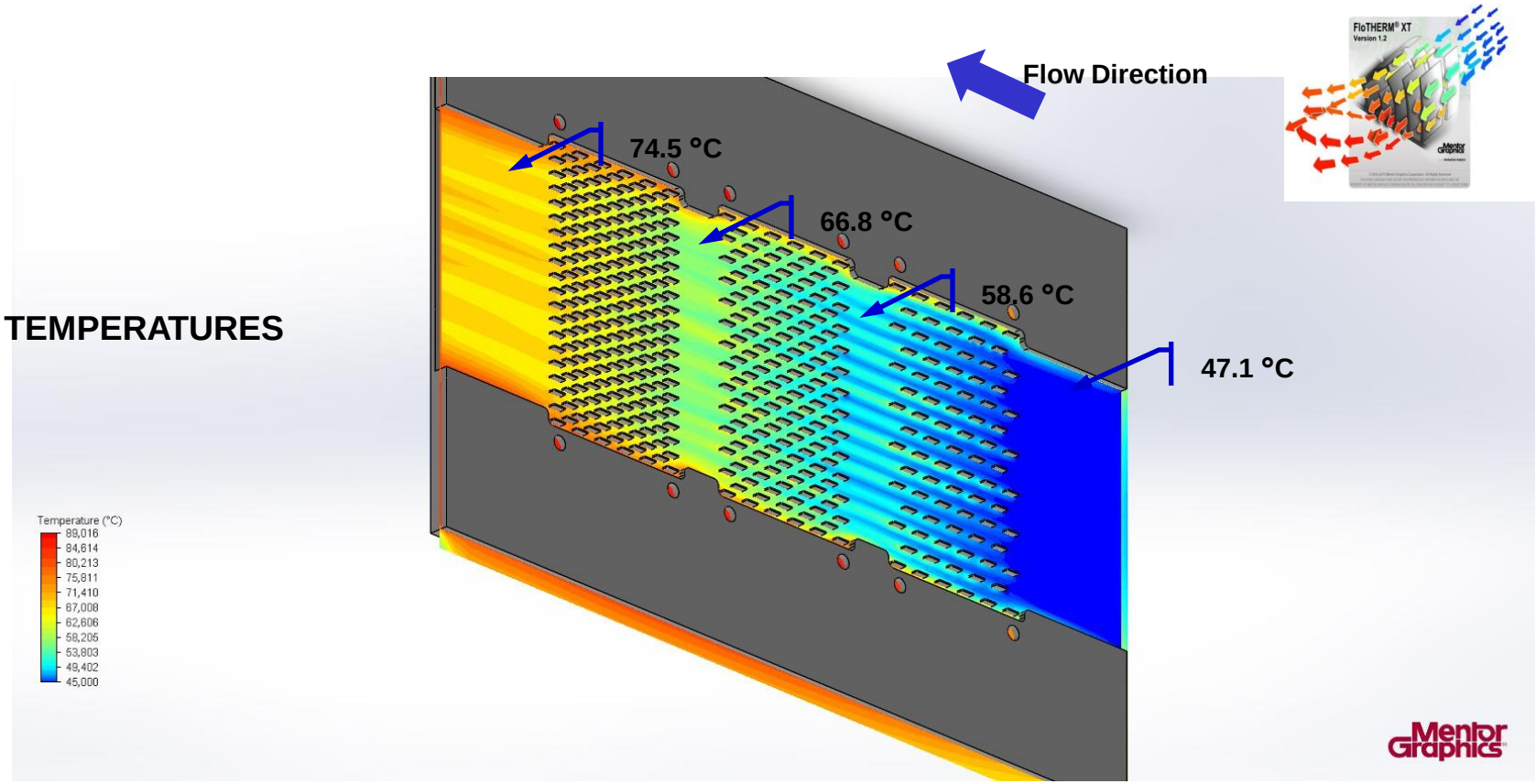
Δ IGBT: 1.4 °C
Δ Diode: 1.1 °C

Mentor Graphics

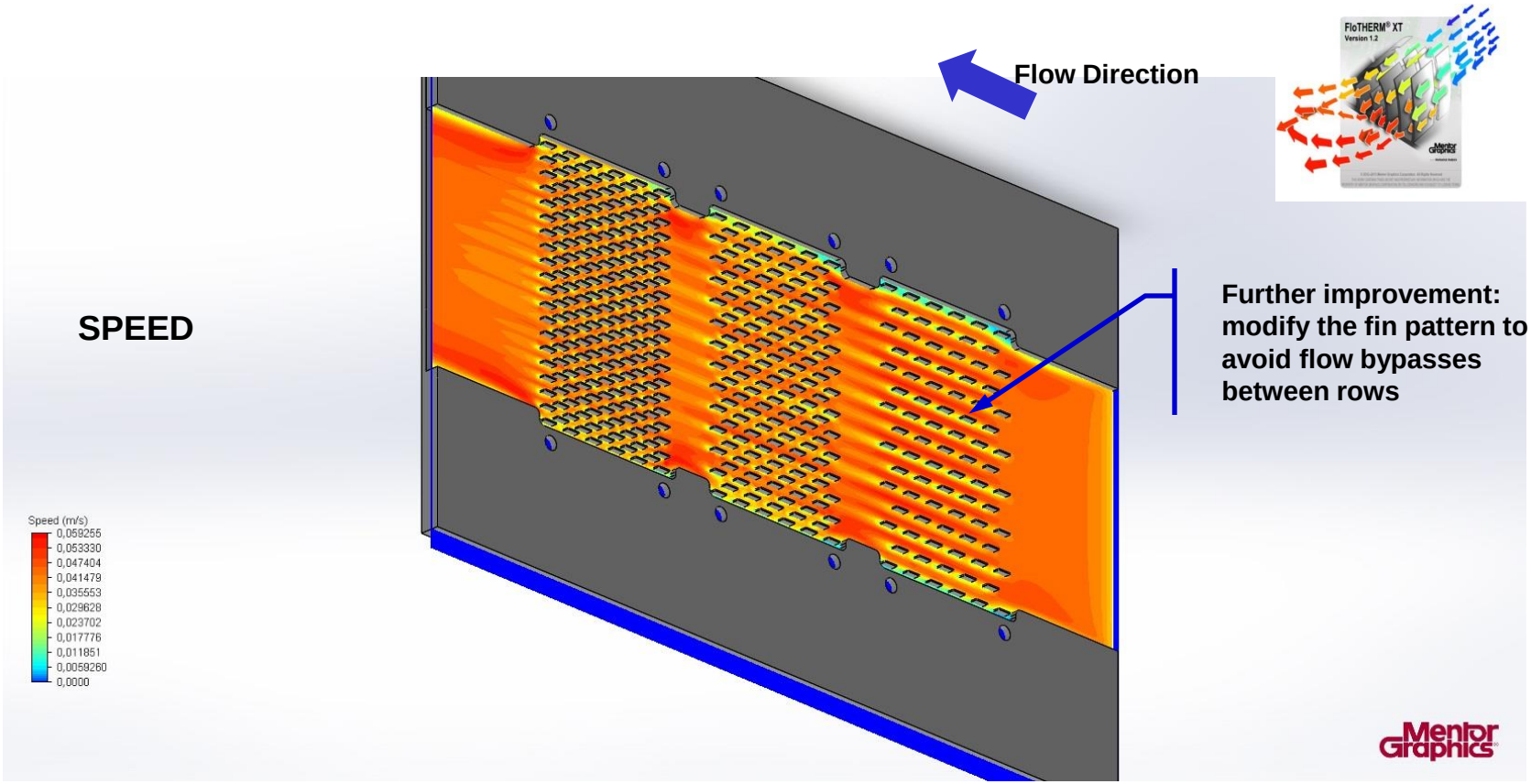
# Example


Diode
Max: 116 °C
Min: 109.5 °C
Flow Direction
IGBT
Max: 116.5 °C
Min: 110.5 °C
IGBT
Max: 117.5 °C
Min: 110.5 °C
IGBT
Max: 118.5 °C
Min: 108 °C
IGBT 3
IGBT 2
IGBT 1
Diode
Max: 118 °C
Min: 107 °C
Diode
Max: 117.5 °C
Min: 110 °C
Solid Temperature (°C)
120,76
116,74
112,72
108,70
104,68
100,67
96,650
92,630
88,610
84,590
80,570
FloTHERM® XT
Version 1.2
Mentor Graphics

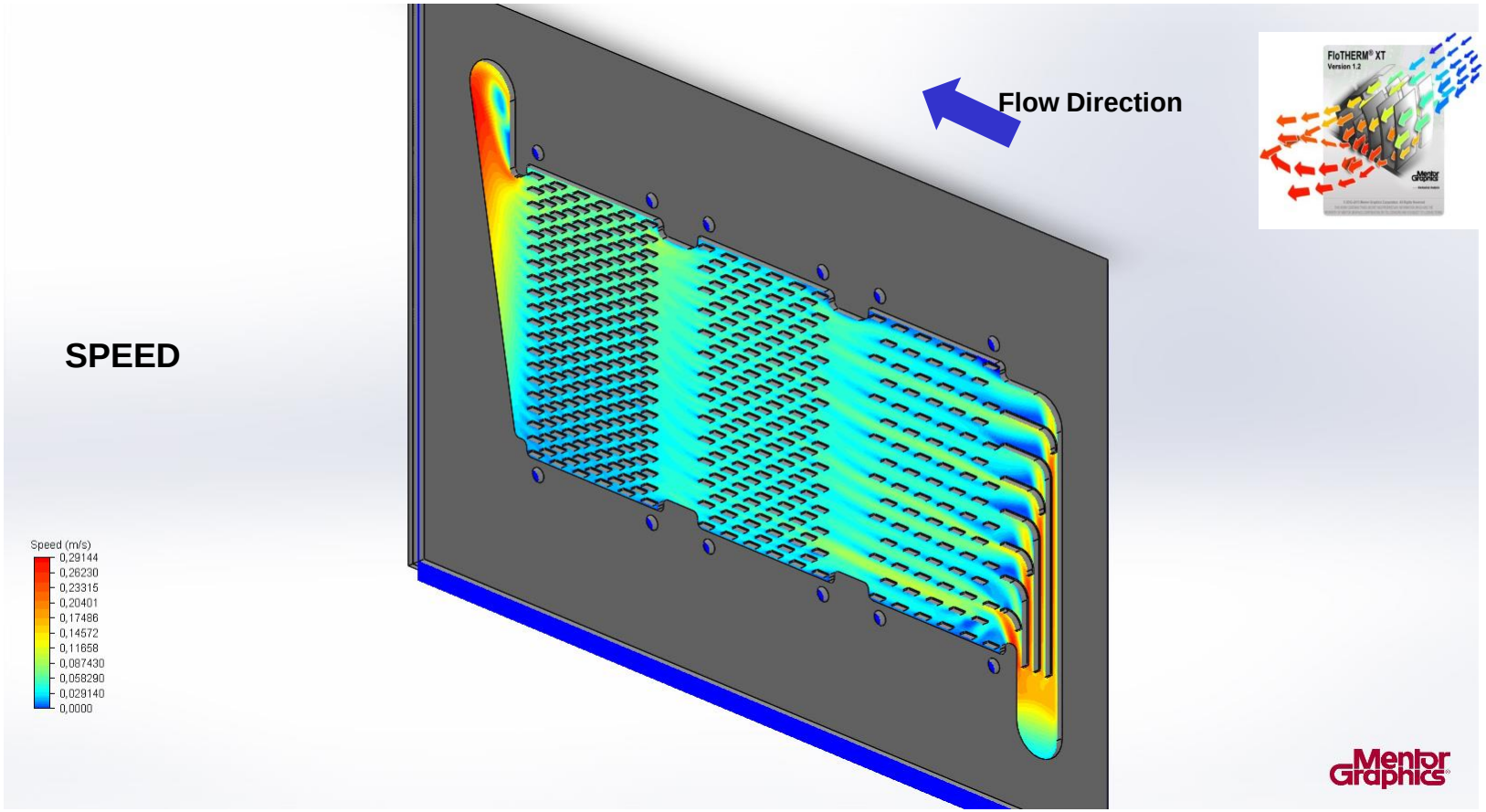
# Example


Flow Direction
74.5 °C
66.8 °C
58.6 °C
47.1 °C
TEMPERATURES
Temperature (°C)
89,016
84,614
80,213
75,811
71,410
67,008
62,606
58,205
53,803
49,402
45,000
FloTHERM® XT
Version 1.2
Mentor Graphics

# Example

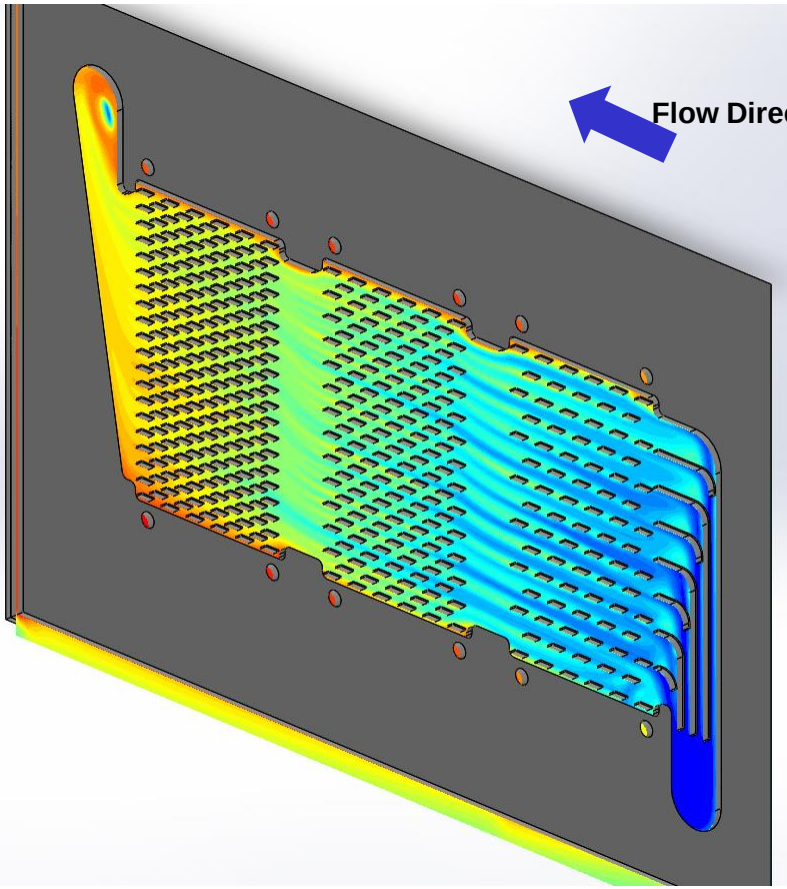

Flow Direction
FloTHERM® XT
Version 1.2
SPEED
Speed (m/s)
0,059255
0,053330
0,047404
0,041479
0,035553
0,029628
0,023702
0,017776
0,011851
0,0059260
0,0000
Further improvement: modify the fin pattern to avoid flow bypasses between rows
Mentor Graphics

# Example


Flow Direction
SPEED
Speed (m/s)
0,29144
0,26230
0,23315
0,20401
0,17486
0,14572
0,11658
0,087430
0,058290
0,029140
0,0000
FloTHERM® XT
Version 1.2
Mentor Graphics

# Example

**TEMPERATURES**

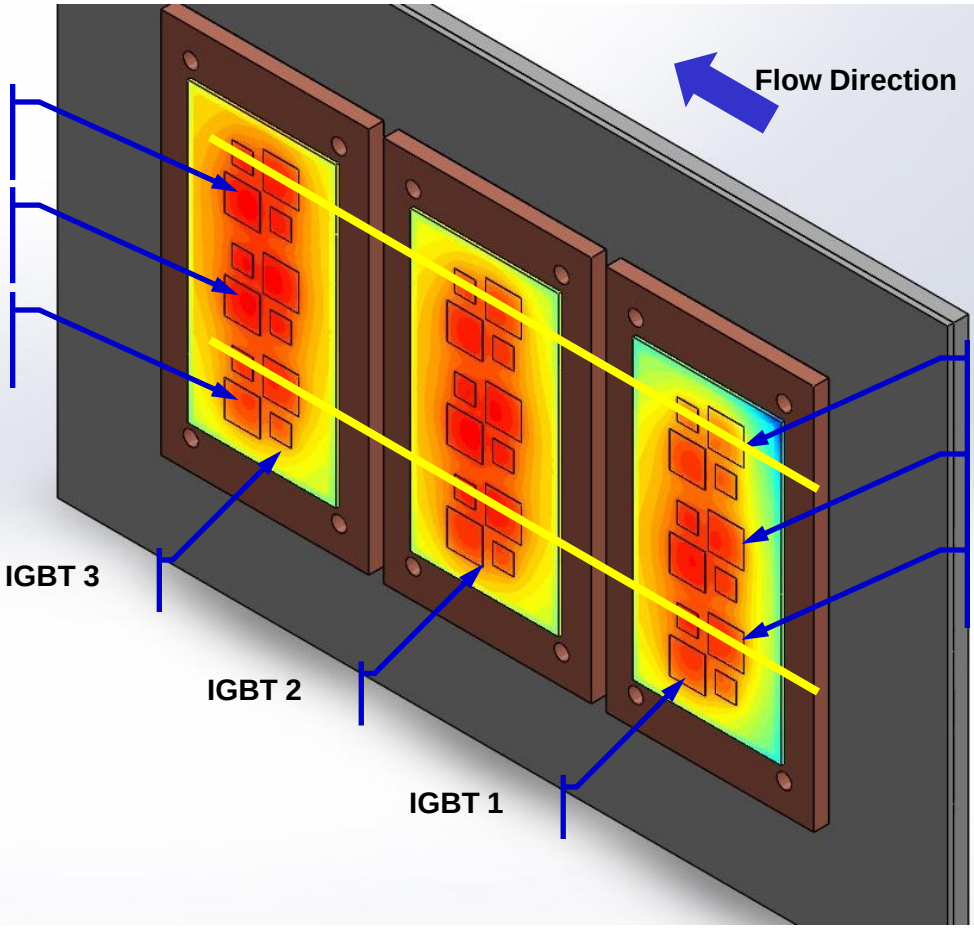



# Example

Δ IGBT: 6.5 °C
Δ Diode: 8.5 °C

Δ IGBT: 1.4 °C
Δ Diode: 3.6 °C

Δ IGBT: 2.5 °C
Δ Diode: 3.5 °C





Δ IGBT: 12.3 °C
Δ Diode: 10.1 °C

Δ IGBT: 5.2 °C
Δ Diode: 2.7 °C

Δ IGBT: 3.1 °C
Δ Diode: 2.1 °C

# Conclusion

- We demonstrated by applying a simple process that it is possible to lower temperature difference between identical chips with a serial cooling scheme
  - We manage the Rth for each component
- This has to be made in conjunction with:
  - A chip layout avoiding temperature gradient
  - An incoming flow evenly distributed on the all width of the heat sink